REMARKS

Claims 1-23 are presented for prosecution. No claim is amended. No claim is cancelled.

Claims 1-5, 7-12, 14-19, and 21-23 are rejected under 35 USC 102(b) as being unanticipated by Zietlow et al. Claims 6, 13, 20 are rejected under 35 USC 103(a) as being unpatentable over Zietlow et al. in view of Mikkelsen et al.

Firstly, Applicants point out that in Applicant's previous Remarks, filed on November 23, 2005, Applicants noted several claim limitations in direct conflict with the teachings of Zietlow et al. The current Office Action continues to reject current claims under 35 USC 102(b) in spite of the noted claim limitations in conflict with Zietlow et al, and further dismisses these claim limitations as mere "design choices". Applicants respectfully put forth that it is improper for the current Office Action to be made Final without providing Applicants with the opportunity to respond to the current Office Action's new grounds of rejections, at least in regards these previously unaddressed claim limitation rejections.

Returning now to the current Office Action, in Item 4 (page 2) of the "Response to Arguments" section of the current Office Action, the Examiner states that he considers the claim limitation specifying a "second memory smaller than said first memory space" to be merely a design choice. Applicants respectfully disagree since this difference in memory space is at the heart of the problem being solved by the present invention. If the two memory spaces were of equal size, then there would be no reason for parsing one memory into tiles, and transferring the tiles, in turn, to the second, smaller memory.

As it is known in the art, differences in the memory size of different devices that can lead to incompatibility issues is a fact of life, and a physical constraint that must be accepted and dealt with. One does not chose to design incompatibility issues into integral components of a system. For example, a computing device's hard drive is much larger than the RAM memory the computer device uses for active calculations. This is not by choice, but by physical and practical constraints. For example, today's hard drives may have

hundreds of gigabits of memory and be very compact in size, but a RAM memory of equal capacity would be impractically huge in physical size and far more expensive. This is a primary reason why computers use large capacity hard drives for archival operations, and comparatively small capacity RAM for active operations.

Similarly, single-user printers typically include a limited amount of solid-state memory for active operations, but do not include a hard drive. An image that fully fits on a computer's hard drive, may not fully fit in the printer's solid-state memory. This is not a design choice. Since a hard drive may cost more than twice that of a typical single-user printer, it is impractical to assume that not incorporating a hard drive (of equal size as the computer's hard drive) into a single-user printer is a mere "design choice". Incorporating such a hard drive into the single-user printer would likely triple the cost of the printer, and have only limited use within the printer since printers do not maintain archives of printed paged. Thus, Applicants asserts that is it improper to assume that the problem being solved by an invention (i.e. the issue of two dissimilar memory spaces) is a design choice.

In Item 5 of the "Response to Arguments" section of the current Office Action, states that data is divided into rows and columns, and the "fact that the divisions of the image are predefined does not mean that they do not undergo a sub-division algorithm". Applicants respectfully point out that the presently claimed invention does not recited divided data (i.e. data that was divided sometime in the pass, and fixed in divided form). Rather, the present invention recites a "data processing unit" applying a sub-dividing algorithm to said target image to generate an array of rows and columns of sub-image tiles. This sub-division is thus required to be done in real-time and to every print image. This is clearly different from a *fixed* printing pattern for letters and symbols. Furthermore, nowhere does Zietlow et al. teach or suggest a "data processing unit" for apply*ing* such a sub-dividing algorithm to each image to be printed.

In Item 6 of the "Response to Arguments" section of the current Office Action, the Office Action asserts that bit pattern memory A and bit pattern page B are connected by the page rotation module. (Applicants request that the

Examiner identify the page rotation module being referred to here, since Fig. 2 shows that the bit pattern memory A and bit pattern page B are inside the page rotation device and not in communication with each other through a page rotation module.) The Office Action further states:

> "Further Zietlow et al discloses in column 3, lines 24-30; 'The write address logic unit WAL and the read address logic unit RAL are in communication with the two bit pattern page memories A and B through the common memory control unit MC, and function to drive the bit pattern page memories such that one of the memories A and B is in the read mode while the other is in its write mode.' Using the broadest reasonable interpretation allowable it is possible that information is passed from one page memory location to the second location based on the assumption that one is reading information while the other is writing information."

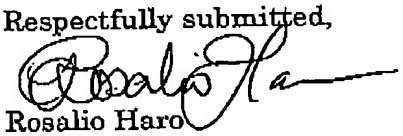
Applicants respectfully put forth that such an interpretation is not allowable. Firstly, the WAL and RAL units, are merely the memory control circuitry for the two-port memory constituted by the two bit pattern page memories A and B. The WAL and RAL units themselves do not read or write to bit pattern page memories A and B and thus cannot be assumed to act as links between them. That is, (please refer to Zeitlow et al.'s Fig. 2) the WAL unit controls one of bit pattern page memories A or B to place it in a write mode via input driver P1 (for page memory A) or input driver P2 (for page memory B), while the RAL unit controls the other of bit pattern page memories A and B to place it in a read mode via output driver P3 (for page memory A) or output driver P4 (for page memory B). Fig. 2 clearly shows no link (or loop) from page memory A to page memory B, or from link page memory B to page memory A.

In reference to Item 7 of the "Response to Arguments" section, the Office Action notes that, "The applicant further points out that data should be transferred in turn from the first memory location to the second." However, the "Examiner believes that the applicant is again exercising design choice. The first and second memory spaces are of equal size it is entirely plausible that whatever information fits in the fist memory location will fit in the second memory location. The examiner believes it is equally effective to transfer the image in larger groups that transfer the image in tiles in turn. Further, the applicant does not disclose in the Remarks what advantage is gained by loading data in

turn... ." Applicants again assert that a problem being solved by the present invention is *how to print when two memories are not of equal size*, and the benefit of the present invention is that the image in the larger memory can be successfully printed using the smaller second memory. Stated differently, sending tiles in turn is not a design choice because having two memories of dissimilar size is not a design choice.

Entry of this Response After Final Rejection, as an earnest attempt to advance prosecution and reduce the number of issues, is respectfully requested. Should the Examiner believe that issues remain outstanding, he is respectfully requested to contact applicants' undersigned attorney in an effort to resolve such issues and advance the case to issue.

Respectfully submitted,



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Date: January 23, 2006